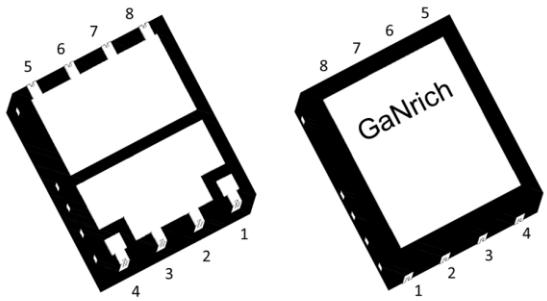
GR-10E001DG: Enhancement Mode Power Transistor

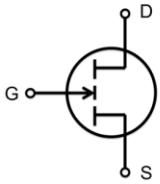
Description

GR-10E001DG is an enhancement mode GaN on Silicon power transistor. 10E001DG provides, high current and high operating speed which is suitable for DC to DC power supply applications.

GR-10E001DG, DFN-5x6-8L



DFN-5x6, Dual side cooling



Drain	5, 6, 7, 8
Source	2, 3
Gate	1, 4

Key Specifications

Part Number	GR-10E001DG
V_{DSS}, min.	100V
$I_{DS,\ Pulse\ (25°C,\ TPULSE\ =\ 300\mu s)}$	307A
$R_{DS(ON),\ typ.\ @VGS=5V}$	1.2mΩ
Q_G, typ.	28nC

Features

- 100V enhancement mode power transistor
- High operating frequency
- R_{DS}(on) = Typ. 1.2 mΩ
- Dual-side cooled package
- HS compliant

Applications

- Switch Mode Power Supplies (SMPS)
- DC-DC Converters
- Fast Battery Charging
- Appliance Motor Drives

1. Electrical Characteristics

➢ Table 1 Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-source voltage	100	V
$V_{(TR)DSS}$	Transient drain to source voltage[a]	120	V
V_{GSS}	Gate- source voltage	-6V ~ +6V	V
I_D	Drain current (continuous) at T_C = 25°C operation	99	A
	Drain current (continuous) at T_C = 100°C operation	68	A
$I_{D,Pulse}$	Pulsed drain current (pulse width: 300μs, Vgs=5V)[b]	307	A
T_J	Operating temperature	-40 to +150	°C
T_S	Storage temperature	-40 to +150	°C
MSL	Moisture sensitivity level	MSL3	

a. In off-state, spike duty cycle D<0.01, spike duration <1μs
b. Defined by product design and characterization. Value is not tested to full current in production

➢ Table 2 Thermal Characteristics

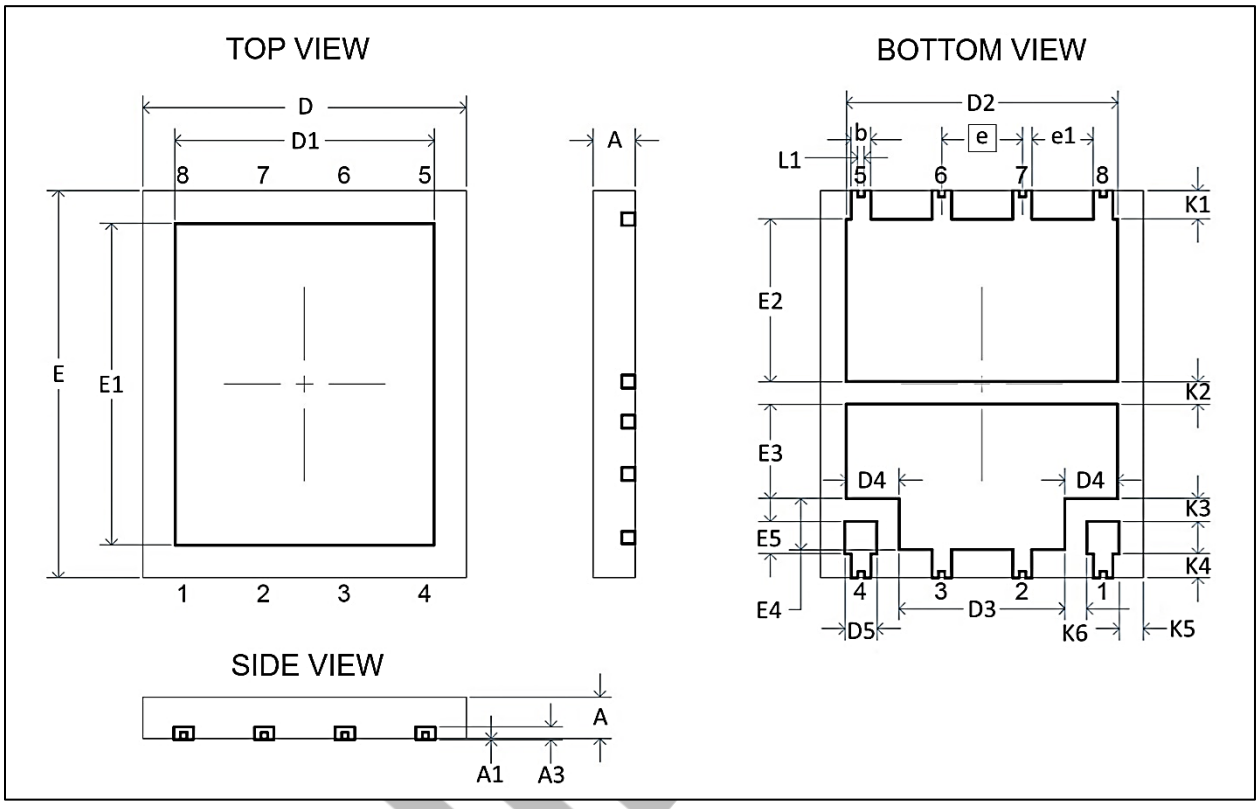
Symbol	Parameter	Value	Unit
$R_{\Theta JC\ (top)}$	Thermal resistance junction-case [a], top	0.30	°C/W
$R_{\Theta JC\ (bottom)}$	Thermal resistance junction-case [a], bottom	0.45	°C/W
$R_{\Theta JA}$	Thermal resistance junction-ambient [b]	60	°C/W

a. Tested in package DFN-5x6.
b. Device on 1 layer PCB.

➢ **Table 3 Electrical Characteristics** (T_{CASE} = 25 °C unless otherwise stated)

Symbol	Parameter	Conditions	Values			Unit
			min.	typ.	max.	
V_{DSS}	Drain-source voltage	V_{GS}= 0V, I_D= 150μA	100	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D= 15mA	0.8	1.1	1.6	V
$R_{DS(on)}$	Drain-source on-resistance	V_{GS}= 5V, I_D= 50A	-	1.2	1.6	mΩ
I_{DSS}	Drain-source leakage current	V_{DS}= 80V, V_{GS}= 0V	-	5.0	400	uA
I_{GSS}	Gate-to-Source Forward Leakage current	V_{GS} = +5V	-	0.19	38	mA
	Gate-to-Source Forward Leakage current	V_{GS} = +5V, T_J=125°C	-	1.5	45	mA
	Gate-to-Source Reverse Leakage current	V_{GS} = -4V	-	0.15	4.5	mA
C_{ISS}	Input capacitance	V_{DS}=50V, V_{GS}=0V	-	4750	-	pF
C_{OSS}	Output capacitance		-	1350	-	
C_{RSS}	Reverse transfer capacitance		-	15	-	
Q_G	Gate charge	V_{DS}= 50V, V_{GS}= 5V, I_D= 50A	-	28	-	nC
Q_{GS}	Gate-source charge	V_{DS}= 50V, I_D= 50A	-	11	-	
Q_{GD}	Gate-drain charge			2.7		
Q_{OSS}	Output charge	V_{DS}= 50V, V_{GS}= 0V	-	110	-	
Q_{RR}	Source-Drain Recovery Charge	-	-	0	-	

2. Package Outline Dimensions (DFN-5x6-8L)



➢ **Table 4 Dimension of GR-DFN-5x6-8L**

SYMBOL	DIMENSION (MM)			SYMBOL	DIMENSION (IN MM)		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.60	0.65	0.70	**E1**	4.977 REF		
A1	--	0.02	0.05	**E2**	2.42	2.52	2.62
A3	0.203 REF			**E3**	1.36	1.46	1.56
D	4.90	5.00	5.10	**E4**	0.69	0.79	0.89
E	5.90	6.00	6.10	**E5**	0.40	0.50	0.60
e	1.25 BSC			**K1**	0.34	0.44	0.54
e1	0.85	0.95	1.05	**K2**	0.25	0.35	0.45
b	0.20	0.30	0.40	**K3**	0.257	0.357	0.457
D1	4.018 REF			**K4**	0.273	0.373	0.473
D2	4.10	4.20	4.30	**K5**	0.275	0.375	0.475
D3	2.468	2.568	2.668	**K6**	0.241	0.341	0.441
D4	0.716	0.816	0.916	**L1**	0.05	0.10	0.20
D5	0.40	0.50	0.60	**-**	-	-	-

3. Change Log

Version	Date	Description
0.1	March 28, 2025	Initial version
0.2	April 16, 2026	Electrical characteristics revised

- **Note:** GaNrich semiconductor reserves the right to revise products and/or specifications without notice.