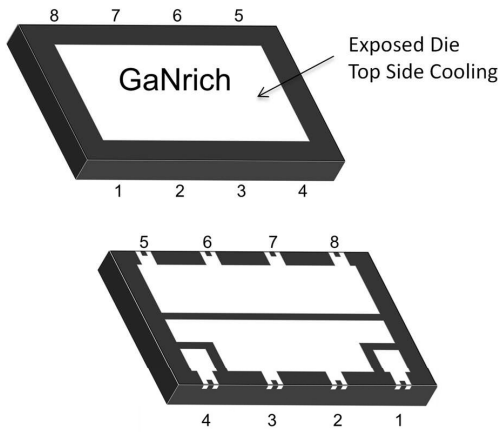
GR-15E007UG: E-mode GaN Power Transistor

Description

GR-15E007UG is an enhancement mode GaN on Silicon power transistor. GR-15E007UG provides, high current and high operating speed which is suitable for DC to DC power supply applications.

GR-15E007UG, DFN-5x3



Drain	5, 6, 7, 8
Source	2, 3
Gate	1, 4

Key Specifications

Part Number	GR-15E007UG
V_{DSS}, min.	150V
$I_{DS,\ Pulse\ (25°C,\ TPULSE\ =\ 300\ \mu s)}$	113A
$R_{DS(ON),\ typ.\ @Vgs=6V}$	7.3mΩ
Q_G, typ.	6.8nC

Features

- 100 V enhancement mode power transistor
- High operating frequency
- RDS(on) = Typ. 7.3 mΩ
- Dual-side cooled package
- HS compliant

Applications

- Switch Mode Power Supplies (SMPS)
- DC-DC Converters
- Fast Battery Charging
- Appliance Motor Drives

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1. Electrical Characteristics

➢ Table 1 Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-source voltage	150	V
$V_{(TR)DSS}$	Transient drain to source voltage[a]	170	V
V_{GSS}	Gate- source voltage	-4V ~ +6V	V
I_D	Drain current (continuous) at T_C = 25°C operation	36.4	A
	Drain current (continuous) at T_C = 100°C operation	25.1	A
$I_{D,Pusle}$	Pulsed drain current (pulse width: 300μs, Vgs=5V)[b]	113	A
T_J	Operating temperature	-40 to +150	°C
T_S	Storage temperature	-40 to +150	°C
MSL	Moisture sensitivity level	MSL3	

a. In off-state, spike duty cycle D<0.01, spike duration <1μs
b. Defined by product design and characterization. Value is not tested to full current in production

➢ Table 2 Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\Theta JC\_Top}$	Thermal resistance junction-case, Top	0.50	°C/W
$R_{\Theta JC\_Bot}$	Thermal resistance junction-case, Bottom	0.50	°C/W
$R_{\Theta JA}$	Thermal resistance junction-ambient	60	°C/W

a. Tested in package DFN 5x3.

➢ **Table 3 Electrical Characteristics** (T_{CASE} = 25 °C unless otherwise stated)

Symbol	Parameter	Conditions	Values			Unit
			min.	typ.	max.	
V_{DSS}	Drain-source voltage	V_{GS}=0V, I_D=200uA	150	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_G =V_D , I_D=3mA	0.8	1.1	1.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}=6V, I_D=20A	-	7.3	9.5	mΩ
I_{DSS}	Drain-source leakage current	V_{GS} =0V, V_{DS} =120V	-	5.0	100	μA
I_{GSS}	Gate-to-Source Forward Leakage current	V_{GS} = 5V, V_{DS} =0V	-	36	650	μA
	Gate-to-Source Forward Leakage current	V_{GS} = 5V, V_{DS} =0V, T_j=125°C	-	900	4200	μA
	Gate-to-Source Reverse Leakage current	V_{GS} = -4V, V_{DS} =0V	-	24	960	μA
C_{ISS}	Input capacitance	V_{GS}= 0V, V_{DS}= 75V	-	578	-	pF
C_{OSS}	Output capacitance		-	280	-	
C_{RSS}	Reverse transfer capacitance		-	10.0	-	
Q_G	Gate charge	V_{GS}=5V, V_{DS}=75V, I_D =20A	-	6.8	-	nC
Q_{GS}	Gate-source charge	V_{DS}= 75V, I_D =20A	-	2.4	-	
Q_{GD}	Gate-drain charge			1.4		
Q_{OSS}	Output charge	V_{GS}= 0V, V_{DS}= 75V	-	36	-	
Q_{RR}	Reverse recovery charge	-	-	0	-	

2- Typical Characteristic Curves

Fig 1. On-Region Characteristics

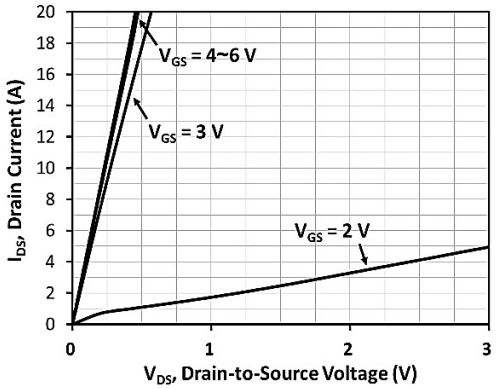


Fig 2. On-Resistance vs Drain Current and Temperature

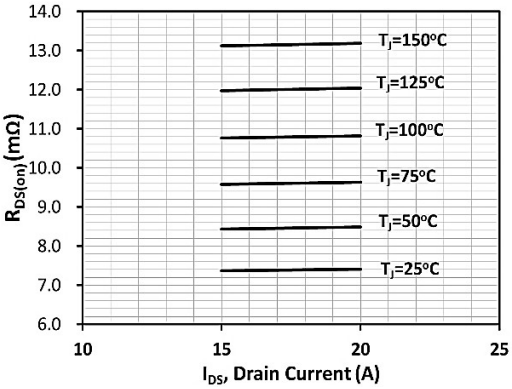


Fig 3. On-Resistance with Drain Current

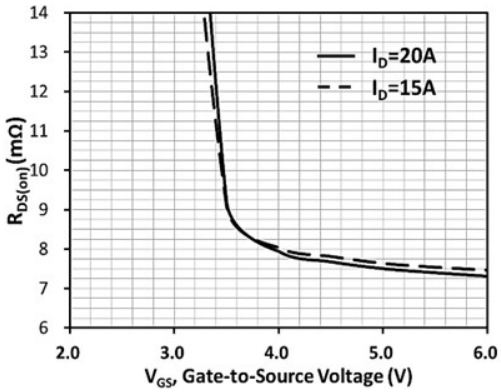


Fig 4. On-Resistance Variation with Temperature

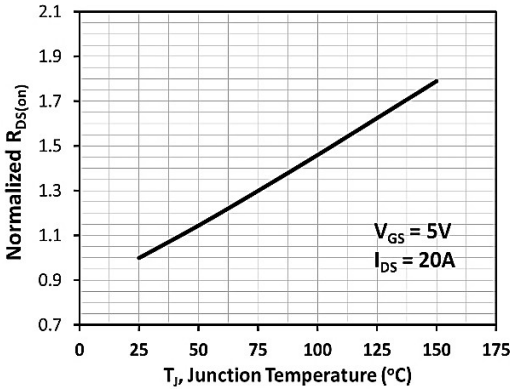


Fig 5. Threshold Voltage with Temperature

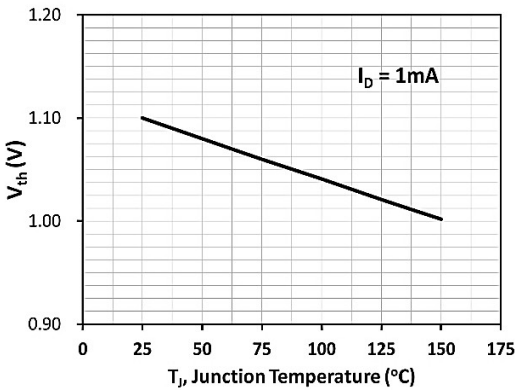


Fig 6. Capacitance Characteristics

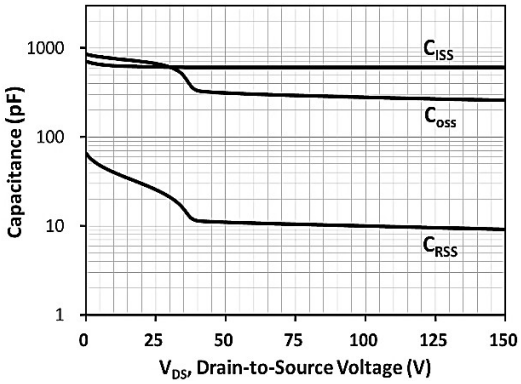


Fig 7. Gate Charge Characteristics, Qg

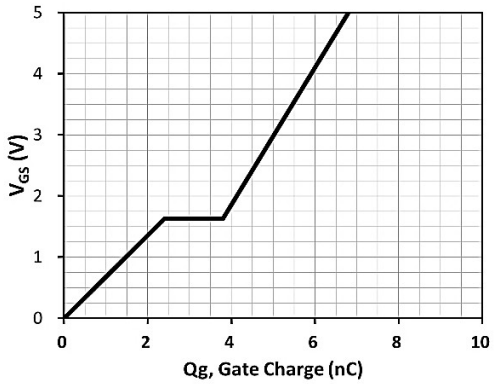


Fig 8. Capacitance Characteristics, Qoss

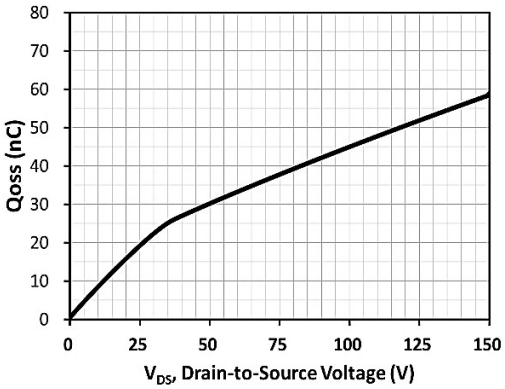
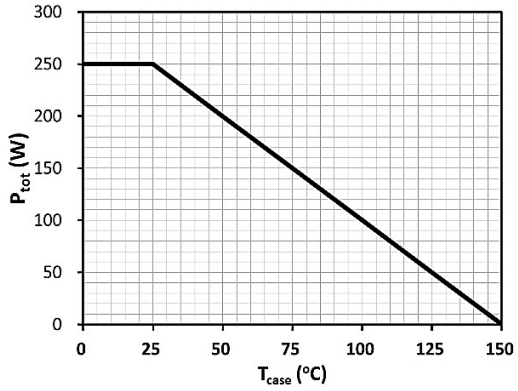
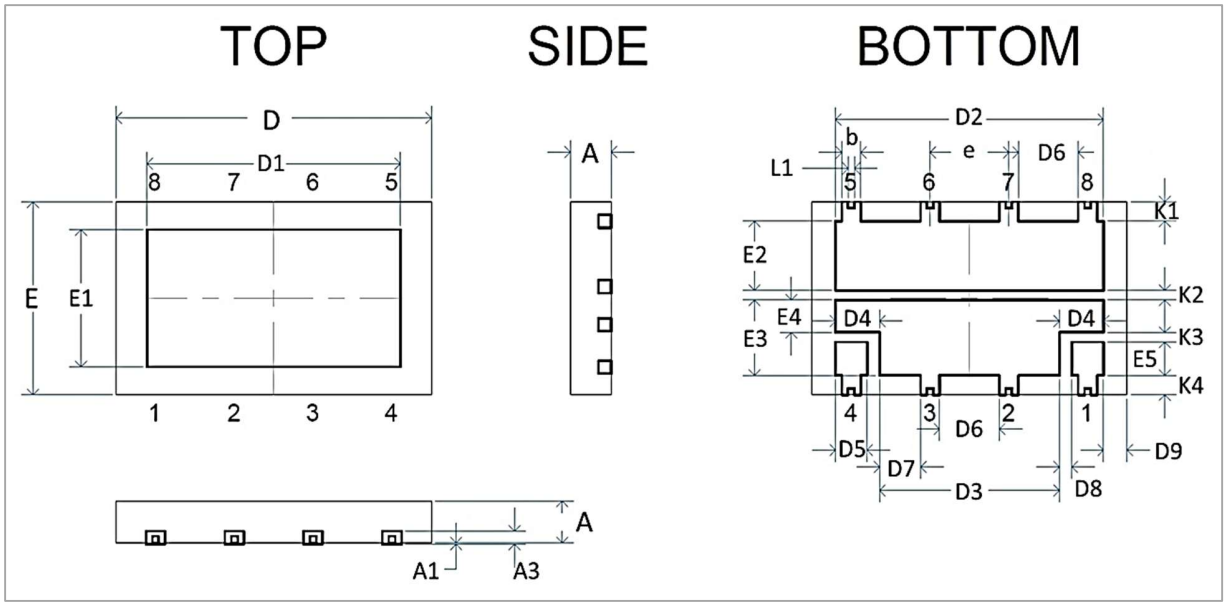


Fig 9. Power Dissipation Derating, Ptot



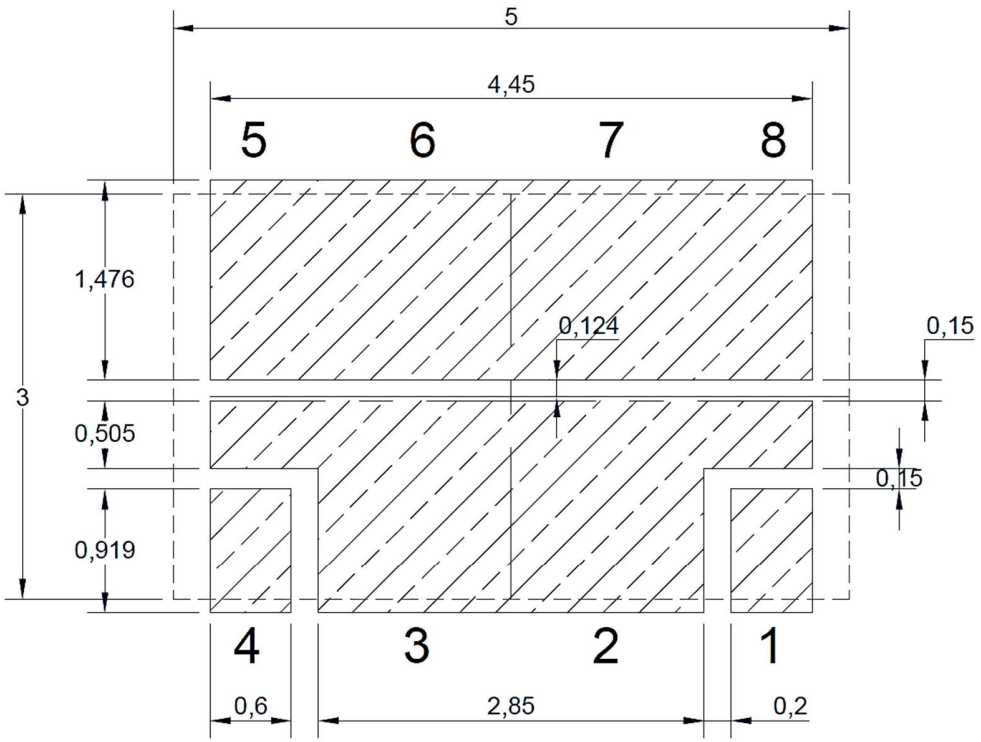
3. Package Outline Dimensions



➢ **Table 4 Dimension of GR-DFN-5x3**

SYMBOL	DIMENSION (MM)			SYMBOL	DIMENSION (IN MM)		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.60	0.65	0.70	**D7**	0.55	0.65	0.75
A2	--	0.02	0.05	**D8**	0.10	0.20	0.30
A3	0.203 REF			**D9**	0.365	0.375	0.385
D	4.90	5.00	5.10	**E1**	2.132 REF		
E	2.90	3.00	3.10	**E2**	0.976	1.076	1.176
e	1.25 BSC			**E3**	1.074	1.174	1.274
b	0.20	0.30	0.40	**E4**	0.405	0.505	0.605
D1	4.018 REF			**E5**	0.419	0.519	0.619
D2	4.15	4.25	4.35	**K1**	0.20	0.30	0.40
D3	2.75	2.85	2.95	**K2**	0.05	0.15	0.25
D4	0.60	0.70	0.80	**K3**	0.05	0.15	0.25
D5	0.40	0.50	0.60	**K4**	0.20	0.30	0.40
D6	0.85	0.95	1.05				

Recommended PCB Soldering footprint

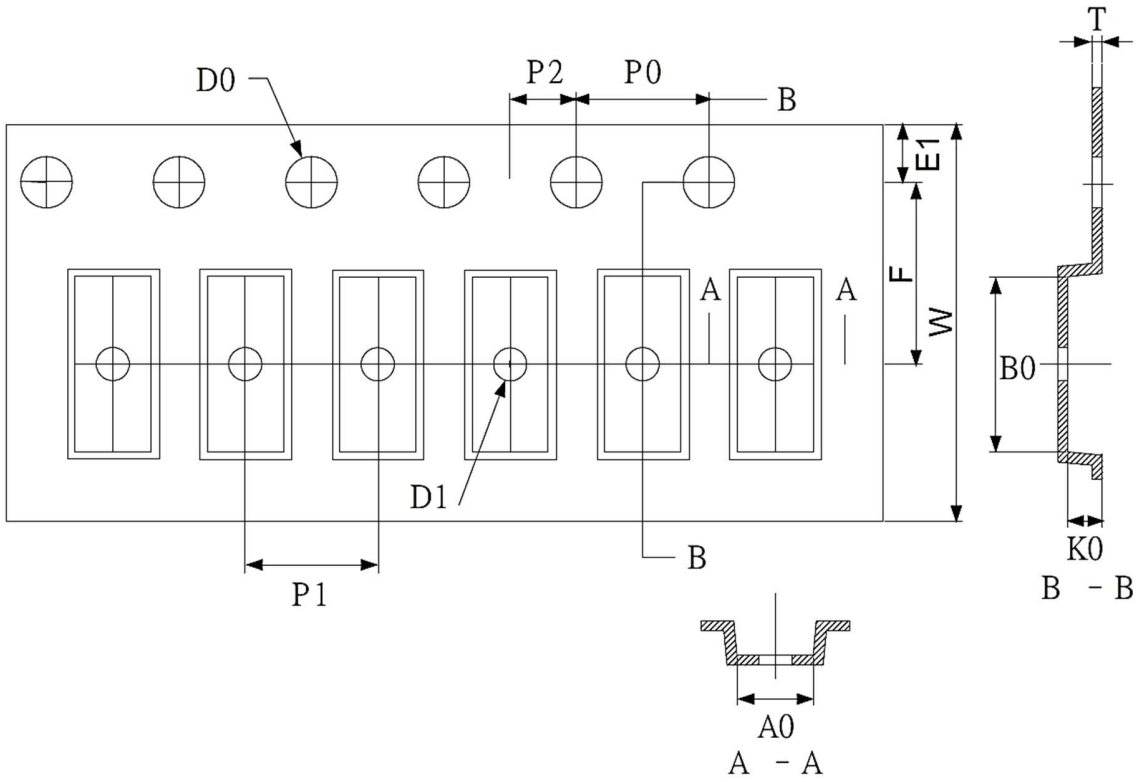


Package outlines

PCB pad openings

4. Tape and Reel Information

13” Reel, Carrier Tape W=12mm



Application	A	H	T1	C	d	D	W	E1	F
DFN 3x5 _EP	180 ± 0.1	50 min.	13.2 ± 0.2	13.0 ± 0.2	1.5 min.	21.0 ± 0.4	12.0 ± 0.3	1.75 ± 0.1	5.5 ± 0.1
Unit: mm	**P0**	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	1.55 ± 0.1	1.0 ± 0.1	0.3 ± 0.05	2.3 ± 0.2	5.3 ± 0.2	1.0 ± 0.1

5. Change Log

Version	Date	Description
0.1	Feb 05, 2025	Initial version
0.2	Sept 26, 2025	Electrical characteristics, Curve information revised.

- ***Note:*** GaNrich semiconductor reserves the right to revise products and/or specifications without notice.