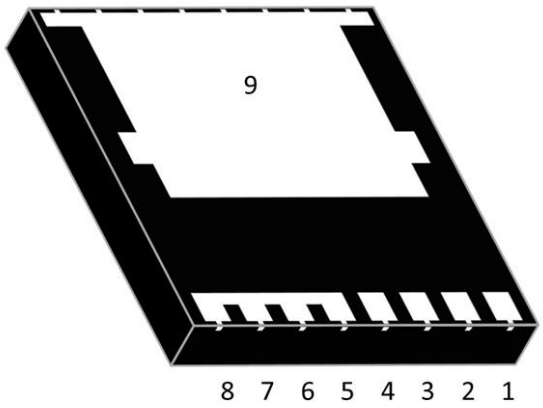
GR-65J150ED: TOLL-9 Cascode GaN HEMT

Description

GR-65J150ED is a normally-off GaN High electron mobility transistor (HEMT) device using the cascode configuration, which provides high breakdown voltage, high current and high operating speed which is suitable for high power applications.

GR-65J150ED (TOLL-9)



Gate: Pin 1
Drain: Pin 9
Kelvin Source: Pin 2
Source: Pin 3 ~ Pin 8

Key Specifications

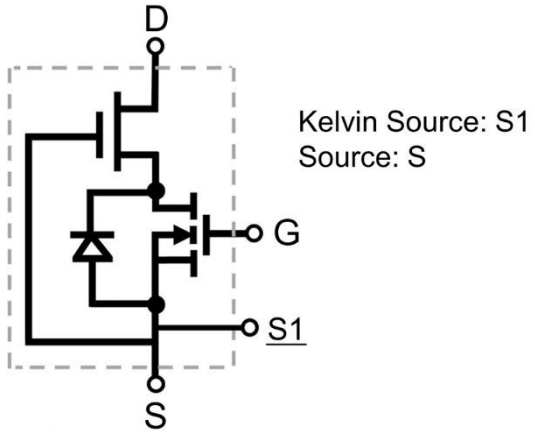
Part Number	GR-65J150ED
V_{DSS}	650V
$V_{(TR)DSS}$	800V
$R_{DS(ON)}$, typ.	149mΩ
Q_G, typ.	11.8nC
Package	DFN 9.9 x 10.5 mm

Features

- Gate drive voltage compatibility (-20V to +20V)
- High operating frequency
- Low Qrr
- ESD-resistant
- Comply with JEDEC standards

Applications

- Switch Mode Power Supplies (SMPS)
- AC-DC/ DC-DC Converters
- Motor Drives



Cascode Device Structure

1- Electrical Characteristics

➢ Table 1 Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-source voltage		650	V
V_{GSS}	Gate- source voltage		-20V ~ +20V	V
I_D	Drain current (continuous) at T_C = 25°C operation		14.5	A
	Drain current (continuous) at T_C = 100°C operation		9.2	A
$I_{D,pulse}$	Pulsed drain current (pulse width: 10μs)		54.4	A
P_D	Maximum power dissipation Tc=25 °C		66	W
T_c	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Soldering peak temperature[b]		260	°C

a. In off-state, spike duty cycle D<0.01, spike duration <1μs
b. For 10 sec., 1.6mm from the case

➢ Table 2 Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\Theta JA}$	Thermal resistance junction-ambient	63	°C/W
$R_{\Theta JC}$	Thermal resistance junction-case	1.9	°C/W

➢ Table 3 ESD Rating

Symbol	Reference	Value	Unit
HBM (G-S) (G-D)	ANSI/ESDA/JEDEC JS-001-2024	2000	V
HBM (D-S)	ANSI/ESDA/JEDEC JS-001-2024	8000	V

➢ **Table 4 Electrical Characteristics** (T_{CASE} = 25 °C unless otherwise stated)

Symbol	Parameter	Conditions	Values			Unit
			min.	typ.	max.	
$V_{(BL)DSS}$	Drain-source voltage	V_{GS}=0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{GS}=V_{DS} , I_D=1mA	2.0	3.0	4.0	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}=10V, I_D=5A, T_J=25 °C	-	149	183	mΩ
		V_{GS}=10V, I_D=5A, T_J=150 °C	-	268	-	
I_{DSS}	Drain-source leakage current	V_{GS} =0V, V_{DS} =650V, T_J=25°C	-	2.5	50	μA
		V_{GS} =0V, V_{DS} =650V, T_J=150°C	-	10	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS}=20V	-	-	100	nA
	Gate-to-source reverse leakage current	V_{GS}=-20V	-	-	-100	
C_{ISS}	Input capacitance	V_{GS}=0V, V_{DS}=400V, f=1MHz	-	658	-	pF
C_{OSS}	Output capacitance		-	17.5	-	
C_{RSS}	Reverse transfer capacitance		-	1.12	-	
Q_G	Gate charge	V_{GS}=0~10V, V_{DS}=400V, I_{DS} =5A	-	11.8	-	nC
Q_{GS}	Gate-source charge			3.2		
Q_{GS}	Gate-drain charge		-	2.0	-	
Q_{OSS}	Output charge	V_{GS}=0V, V_{DS}= 0~400V	-	30.5	-	
$t_{D(on)}$	Turn-on delay time	V_{DS}=400V, V_{GS}=0 to 10V, I_{DS}=2A ,R_G=25Ω	-	8	-	ns
$t_{D(off)}$	Turn-off delay time		-	13	-	
Q_{RR}	Reverse recovery charge	Is=5A, V_{DS} =400V	-	6.0	-	nC

2- Typical Characteristic Curves

Fig 1. On-Region Characteristics

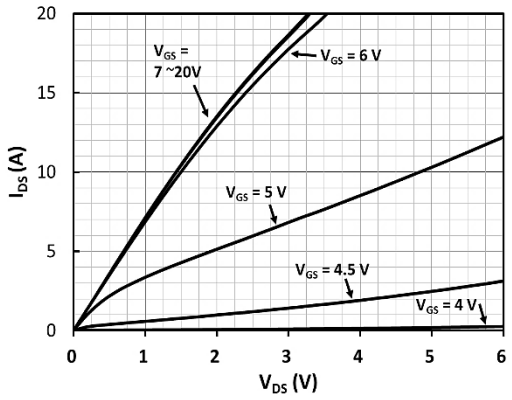


Fig 2. On-Resistance vs Drain Current and Temperature

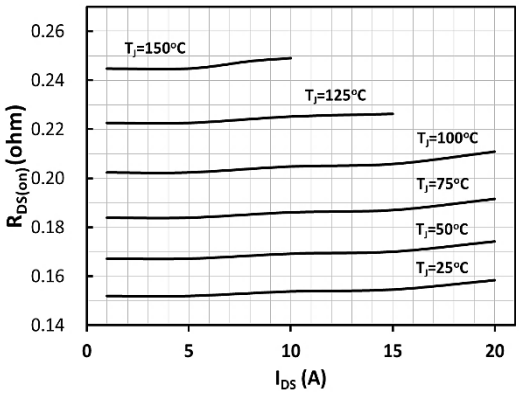


Fig 3. On-Resistance with Drain Current

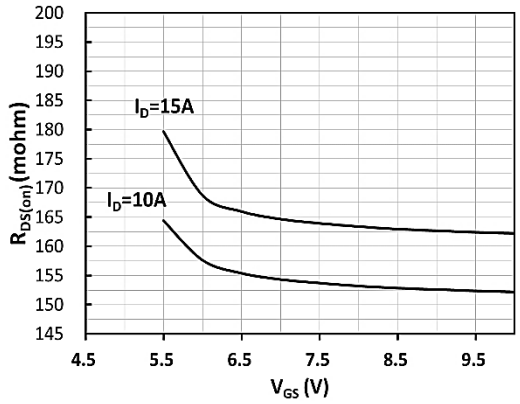


Fig 4. On-Resistance Variation with Temperature

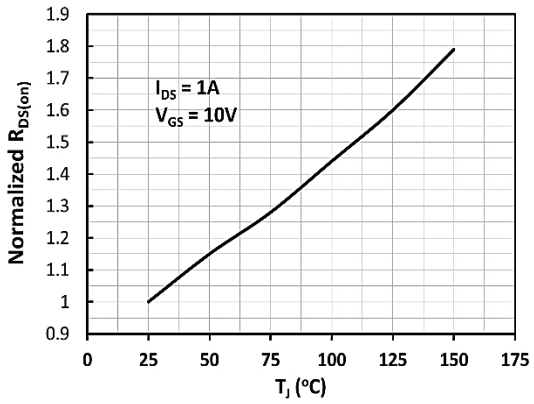


Fig 5. Threshold Voltage with Temperature

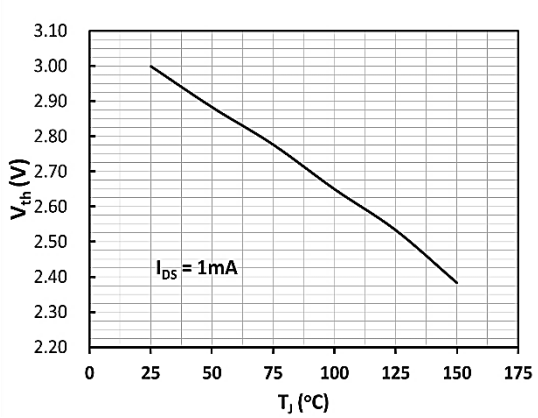


Fig 6. Capacitance Characteristics

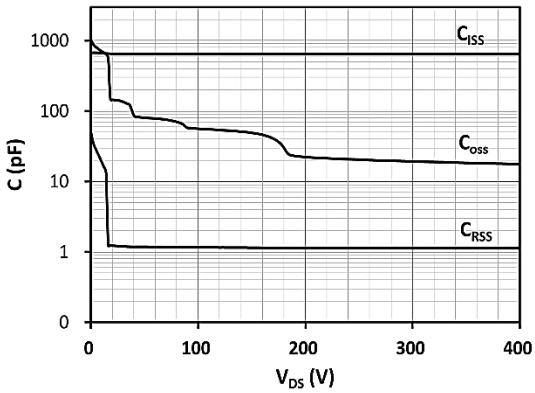


Fig 7. Gate Charge Characteristics, Qg

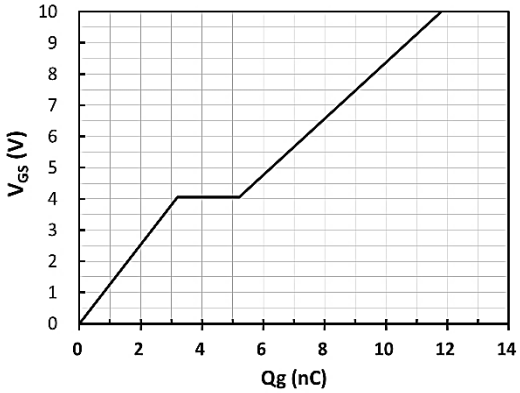


Fig 8. Capacitance Characteristics, Qoss

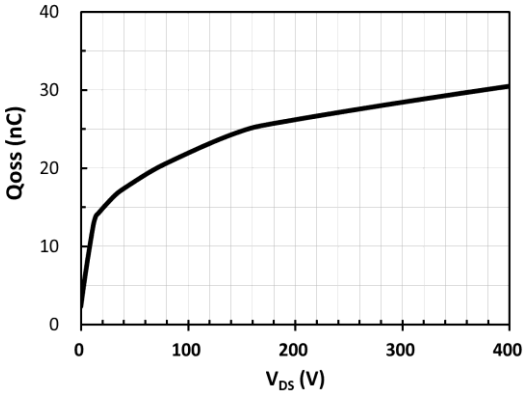
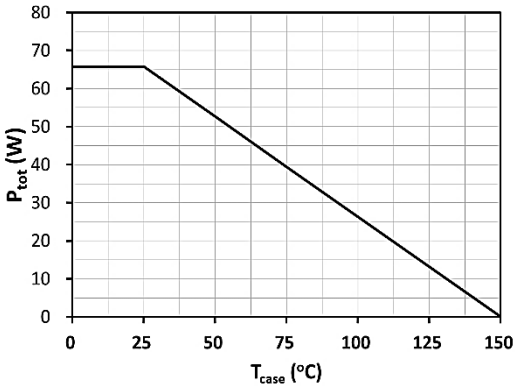
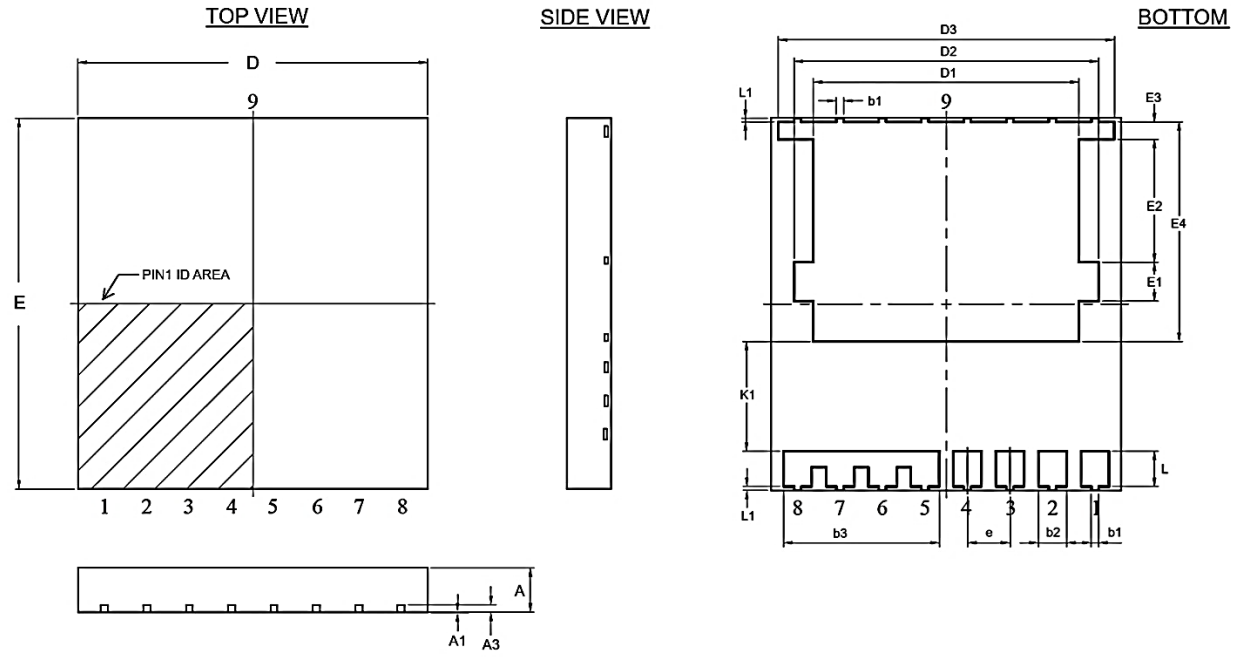


Fig 9. Power Dissipation Derating, Ptot



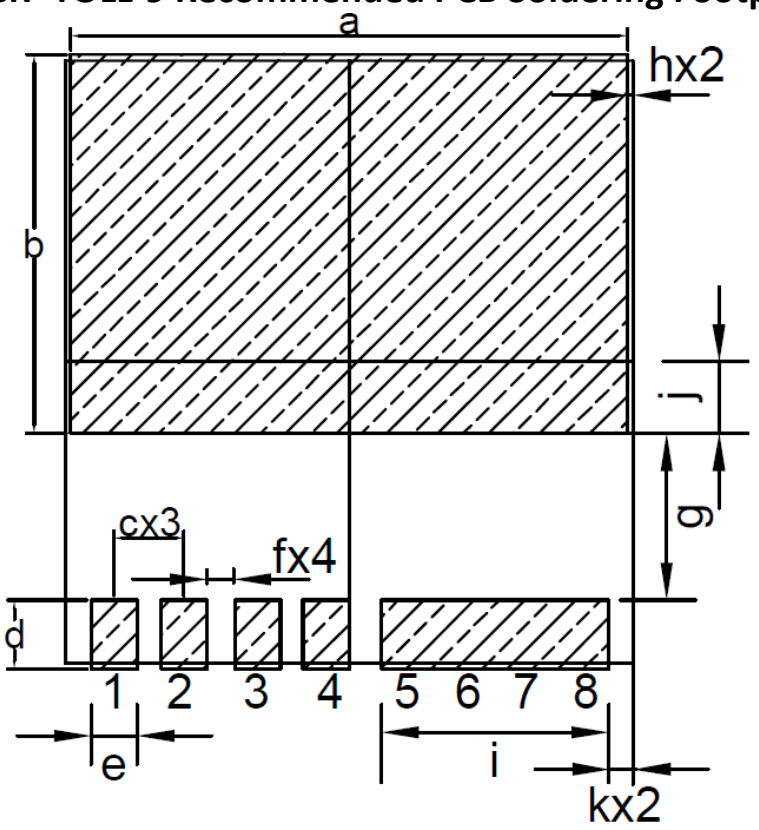
3- Package Outline Dimensions, GR- TOLL-9



➢ **Table 5 Dimension of GR -TOLL-9**

SYMBOL	DIMENSION (MM)			SYMBOL	DIMENSION (IN MM)		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	1.20	1.25	1.30	**E3**	0.40	0.50	0.60
A1	--	0.02	0.05	**E4**	6.10	6.20	6.30
A3	0.203 REF			**L**	1.00	1.10	1.20
D	9.80	9.90	10.0	**L1**	0.10 REF		
D1	7.40	7.50	7.60	**K1**	3.00	3.10	3.20
D2	8.50	8.60	8.70	**b1**	0.20 REF		
D3	9.40	9.50	9.60	**b2**	0.70	0.80	0.90
E	10.4	10.5	10.6	**b3**	4.30	4.40	4.50
E1	1.00	1.10	1.20	**e**	2.10 BSC		
E2	3.37	3.47	3.57	--	--	--	--

GaNrich DFN- GR -TOLL-9 Recommended PCB Soldering Footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	9.70	g	2.90
b	6.60	h	0.10
c	1.20	i	4.40
d	1.20	j	1.25
e	0.80	k	0.35
f	0.40		

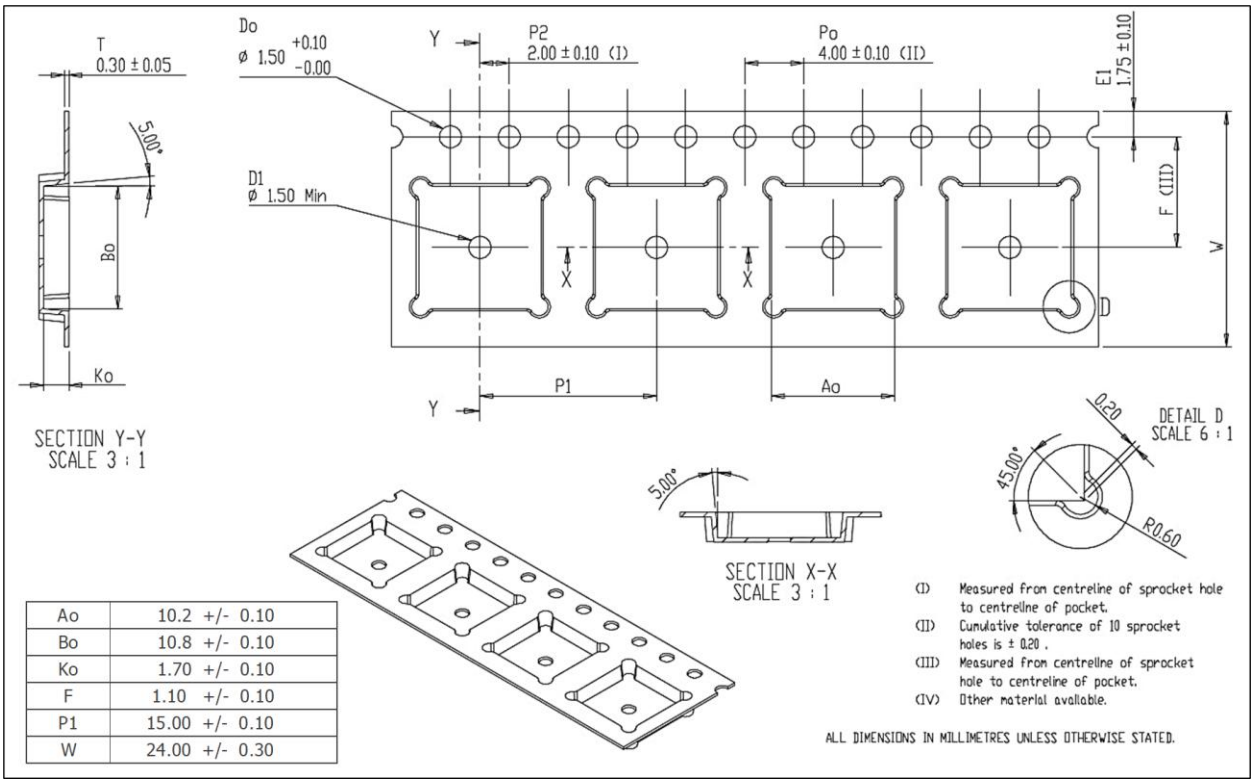
Notes :
(1) All dimension in millimeters.
(2) Drawing not to scale.

Package outlines

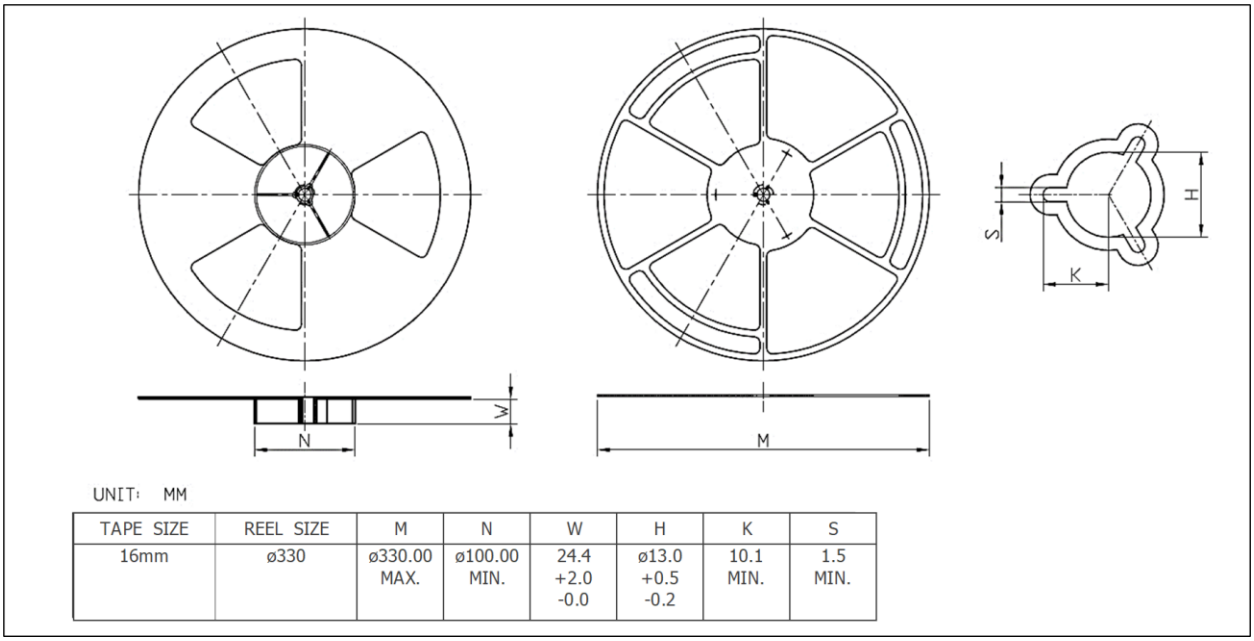
PCB pan openings

*According to **IPC (IPC-A-610)**, solder voids are considered to be a defect when the overall calculated area of all voids in any given solder ball/joint is greater than 25% of the total solder ball area.

4- Tape and Reel Information



Ao	10.2 +/- 0.10
Bo	10.8 +/- 0.10
Ko	1.70 +/- 0.10
F	1.10 +/- 0.10
P1	15.00 +/- 0.10
W	24.00 +/- 0.30



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	H	K	S
16mm	ø330	ø330.00 MAX.	ø100.00 MIN.	24.4 +2.0 -0.0	ø13.0 +0.5 -0.2	10.1 MIN.	1.5 MIN.

5- Change Log

Version	Date	Description
01	September 2, 2024	Initial version
02	February 17, 2025	Add Characteristic Curve
03	April 16, 2026	Electrical characteristics revised

- ***Note:*** GaNrich semiconductor reserves the right to revise products and/or specifications without notice.